SAMPLE CASE · DIAGNOSTIC SPRINT

Design Competition: Truepath Expert vs AI Agents

Same 8-zone alumina heater · Same AI tools · Wafer at 150 °C, 1 and 10 torr
Same methodology calibrated to $R^2 > 0.9$ on more than 30 thermocouples on previous builds

Truepath™

MODEL Steady 3-D conduction with Joule heating, gas-gap conduction plus radiation, temperature-dependent properties.

THE RISK YOU ALREADY CARRY

Unknown questions, unknown answers: the gap even AI didn't close

THE COMPETITION

A team of AI design and manufacturing engineers competed against a similar team led by a Truepath expert, who directed each iteration. Same model, scoring and 120 variation cases.

What did the expert see that AI didn't?

WHERE EXPERT DIRECTION MADE THE DIFFERENCE

1. Which design rules are real process limits, and which are habit?
2. How much uniformity am I giving up to conservative defaults?
3. Does my layout still hit spec once print thickness, shrink and tilt vary in production?
4. Are my feeds, vias and sensor pockets properly simulated, or will they cost me uniformity later?
5. Is my design ready to build, or am I about to pay for a prototype to find out?

Which of these can you answer with confidence today?

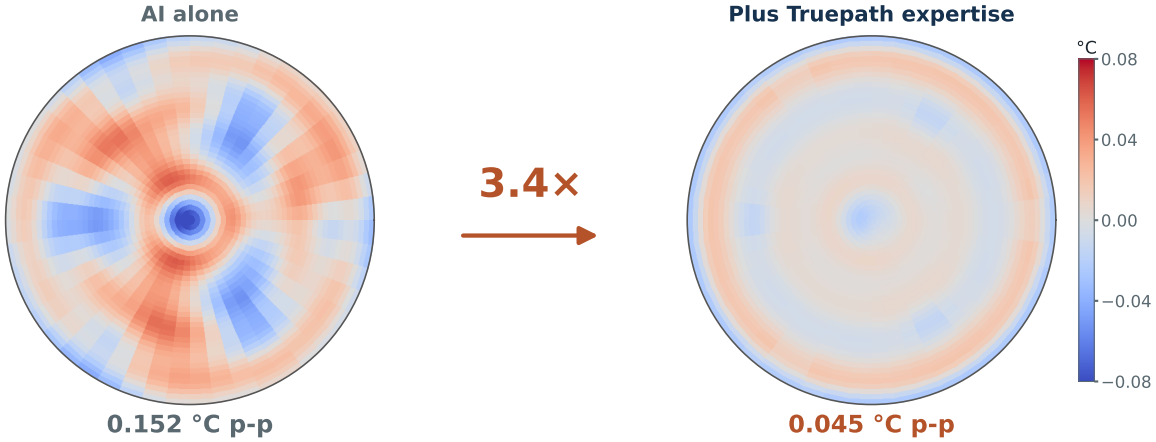
RESULTS (SIMULATED)

0.045 °C
p-p at 1 torr, ideal build
(AI alone 0.152 °C)

0.092 °C
p-p at 10 torr, ideal build
(AI alone 0.309 °C)

3.4×
more uniform wafer, ideal build, 1 and 10 torr

WAFER TEMPERATURE, 1 TORR, IDEAL BUILD (SIMULATED)



Wafer temperature minus mean (150 °C), same color scale for both maps. 1 torr N_2, ideal build. p-p = hottest minus coldest point on the wafer.

KEY INSIGHT

With the layout right, the process sets the remaining error: print-thickness variation within a zone (3%, about 2% σ) drives over 90% of it (worst case 0.334 vs AI alone 0.351 °C, 1 torr). With AI alone, its 0.152 °C layout error would have hidden this limit. Print control now decides the yield, found before any build.

KNOWN ASSUMPTIONS

Feeds, vias, braze pads and thermocouples: modeled.
Print thickness: 3% (about 2% σ) random, modeled across 120 cases.
Lift-pin holes: not modeled; offset in layout on previous builds.
Gas gap, emissivity, alumina k(T): not yet test-validated.

DECISION GATE

Prototype now, or fix the process first?

The layout is one step from a first build: turning the power layout into a print-ready trace.
The open risks are print-thickness control and lift-pin holes.
A **Diagnostic Sprint, from $6,500 fixed,** gives you a written risk assessment in 1–2 weeks, before you cut hardware.

Book a 20-minute scope call at truepathcfd.com

Smaller first steps start there too.

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