SAMPLE CASE · DIAGNOSTIC SPRINT

300 mm wafer heater: about 20× more uniform

Generic 8-zone alumina heater · Thin-film deposition at 150 °C · Wafer held to 0.04 °C
Same methodology calibrated to $R^2 > 0.9$ on more than 30 thermocouples on previous builds

Truepath™

MODEL Steady 3-D conduction with Joule heating, gas-gap conduction plus radiation, temperature-dependent properties.

THE RISK YOU ALREADY CARRY

Uneven wafer temperature costs yield. We find the fix before you build.

THE CHALLENGE

Thin-film deposition at 150 °C needs the 300 mm wafer held to 0.04 °C. Before design optimization, this generic 8-zone alumina heater reached 0.86 °C p-p.

We bring the wafer to spec in simulation.

YOUR QUESTIONS, OUR EXPERTISE

1. When test and simulation disagree, is the cause my model, the part or the measurement?
2. Do my boundary conditions capture every real heat loss and hot spot, plus the second-order effects behind them?
3. What does my model leave out, and will it change the answer?
4. How do I hold the wafer to spec at every operating temperature and pressure, not just the one I tuned?
5. What is the fewest sensors, and where, so my controller reads the wafer accurately without added complexity?
6. Which design and process assumptions erode uniformity in testing, and will it survive production tolerance stack-up?

Which of these can you answer with confidence today?

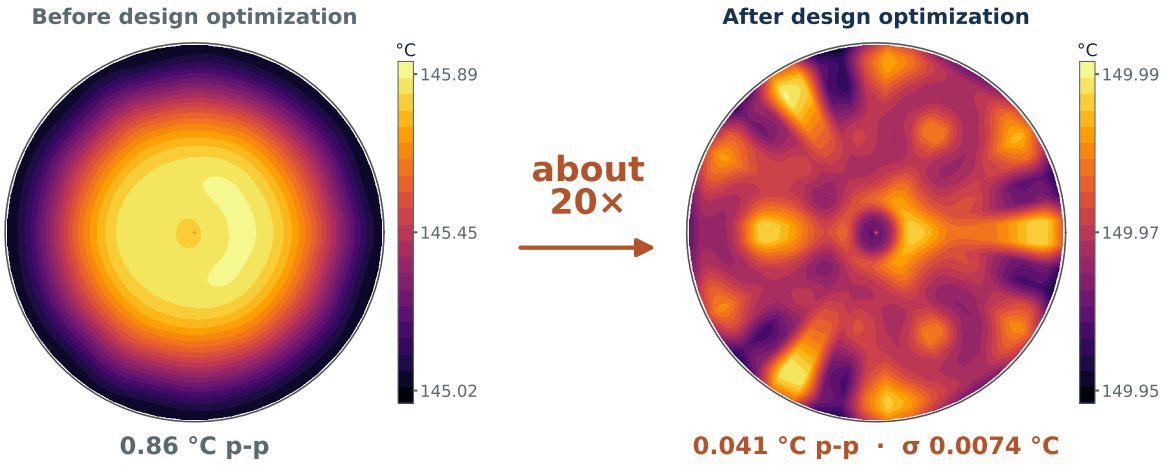
RESULTS (SIMULATED, 300 mm WAFER)

0.044 °C
p-p on a finer mesh, same result, 1 torr

0.074 °C
wafer p-p at 10 torr

0.041 °C p-p ±0.021 °C σ 0.0074 °C
wafer uniformity, p-p, 1 torr

WAFER TEMPERATURE, BEFORE AND AFTER (SIMULATED)



0.86 °C p-p

0.041 °C p-p · σ 0.0074 °C

Circle: wafer edge. 300 mm Si wafer on a 0.1 mm N_2 gap, 1 torr. Each map has its own color scale. p-p = hottest minus coldest point on the wafer.

KEY INSIGHT

Design optimization gains about 20× at 1 torr, which drops to about 11× at 10 torr (0.80 → 0.074 °C). Chamber pressure changes how heat crosses the gap, so uniformity must be proven across the full operating window, not at one setpoint.

KNOWN ASSUMPTIONS (IMPACT ON WAFER P-P)

Trace ripple: a few hundredths of a °C, local (estimate).
Power feeds: modeled; burying them changes p-p by <0.002 °C.
Lift-pin holes: not modeled; offset in layout on previous builds.
Gas gap, emissivity, alumina k(T): not yet test-validated; they shift the radial profile, re-tuned after a TC-wafer test.

DECISION GATE

Prototype now, or look closer first?

The model says 0.041 °C. The open risks are lift-pin holes and your pressure window, and both can be checked in simulation.
A **Diagnostic Sprint, from $6,500 fixed,** gives you a written risk assessment in 1–2 weeks, before you cut hardware.

Book a 20-minute scope call at truepathcfd.com

Smaller first steps start there too.

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